UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,762	02/11/2004	Luis Antonio Basto	AD-346J	3459

7590 02/28/2005

Iandiorio & Teska
260 Bear Hill Road
Waltham, MA 02451-1018

EXAMINER	
RAYMOND, EDWARD	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,762	BASTO, LUIS ANTONIO	
	Examiner	Art Unit	
	Edward Raymond	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040211*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-17** are rejected under 35 U.S.C. 102(e) as being anticipated by Ross et al.

Ross et al. teach a universally accessible fully programmable memory built-in self-test (MBIST) system comprising: an MBIST controller including (Claims 1, 16, and 17: see paragraph 39): an address generator configured to generate addresses for a memory under test (Claims 1, 16, and 17: see paragraphs 39 and 45); a sequencer circuit configured to deliver test data to selected addresses of said memory under test and reading out that test data (Claims 1, 16, and 17: see paragraph 5: The Examiner notes that sequencers are known in the art as stated in the reference); a comparator circuit configured to compare said test data read out of said memory under test to said test data delivered to said memory under test to identify a memory failure (Claims 1, 16, and 17: see paragraph 45), and an externally accessible user programmable pattern register for providing a pattern of test data to said memory under test (Claims 1, 16, and 17: see paragraph 45); and an external pattern programming device configured to

supply a said pattern of test data to said user programmable pattern register (Claims 1, 16, and 17: see paragraph 56).

Ross et al. teach the external programming device includes a computer configured to generate a user defined pattern of test data (Claim 2: see paragraph 56).

Ross et al. teach a system wherein the external programming device includes programmable hardware configured to generate a user defined pattern of test data (Claim 3: see paragraph 56).

Ross et al. teach the system in which the user programmable pattern register includes FLASH memory (Claim 4: see Figure 2: The Examiner notes that Memory 202 performs the function of Flash Memory).

Ross et al. teach the system further including a switch configured to select a computer or programmable hardware to generate a user defined pattern of data (Claim 5: see paragraph 56).

Ross et al. teach a system in which said user programmable pattern register serially receives said test data from said external pattern programming device (Claim 6: see paragraphs 39 and 56).

Ross et al. teach a system in which the user programmable pattern register receives said test data from said external pattern programming device in a parallel configuration (Claim 7: see Figure 2: The Examiner notes that the data is received into the memory in parallel.)

Ross et al. teach a system in which said user programmable pattern register includes from 1 to N bits (Claim 8: see paragraphs 44 and 45: The Examiner notes that digital data is in the form of bits from 1 to N bits).

Ross et al. teach a system in which said user programmable pattern register is located within said MBIST controller (Claim 9: see paragraph 39 and Figure 2).

Ross et al. teach a system in which said user programmable pattern register is located external to said MBIST controller (Claim 10: see Figure 2)

Ross et al. teach a system in which said pattern of test data is an all 0's or an all 1's pattern (Claims 11 and 13: see paragraph 39 and Table 5: The Examiner notes that data stored in the memory for test consists of 1's and 0's).

Ross et al. teach a system in which said pattern of test data is any defined binary data pattern limited only by the size of said user programmable data register (Claim 12: see paragraph 45: The Examiner notes that the data register is limited by the limit of the memory capacity).

Ross et al. teach a system further including a multiplexor where a test mode signal selects said addresses generated from said address generator or system addresses based on a predetermined state of said test mode signal (Claim 14: see paragraph 8).

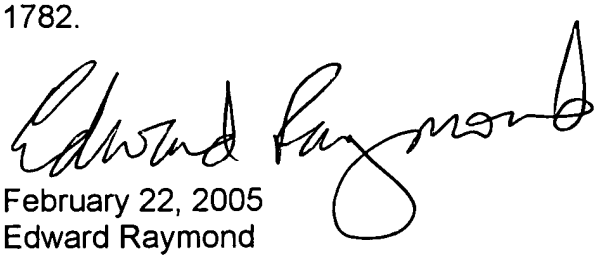
Ross et al. teach a system further including a multiplexor where a test mode signal selects said pattern of test data or system data based on a predetermined state of said test mode signal (Claim 15: see paragraph 8).

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Raymond whose telephone number is 571-272-2221. The examiner can normally be reached on Monday through alternating Friday between 8:00 AM and 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-2221 for regular communications and 571-272-1562 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.



February 22, 2005
Edward Raymond
Patent Examiner
Art Unit 2857